1. A method of forming a split-gate transistor, comprising the steps of:

forming a first polysilicon layer on a substrate which has a plurality of isolation bars formed therein;

forming a plurality of nitride spacers, wherein each spacer is formed over one of the isolation bars, and wherein the plurality of spacers divides the first polysilicon layer into at least one floating gate;

forming a plurality of polysilicon spacers on the nitride spacers;

removing the plurality of nitride spacers;

forming a dielectric layer on the at least one floating gate; and

forming a second polysilicon layer on the dielectric layer, wherein the plurality of spacers divides the second polysilicon layer into at least one control gate.

2. The method of claim 1, further comprising forming source and drain regions in the substrate in a direction orthogonal to said plurality of nitride spacers.

3. The method of claim 1, further comprising forming a tunneling oxide layer on the substrate prior to said step of forming a first polysilicon layer.

4. The method of claim 1, wherein said step of forming a first polysilicon layer comprises chemical vapor deposition.

5. The method of claim 1, wherein said step of forming a first polysilicon layer comprises plasma deposition.

6. The method of claim 1, wherein said step of forming a plurality of nitride spacers comprises defining trenches in the first polysilicon layer and filling the trenches with nitride.

7. The method of claim 1, wherein the at least one floating gate has a thickness of approximately 200 to 1000 Angstroms.

8. The method of claim 1, wherein the at least one floating gate has a thickness of approximately 500 Angstroms.

9. The method of claim 1, wherein the dielectric layer is a layer of ONO.

10. The method of claim 9, wherein said step of forming a dielectric layer comprises formation of a first oxide layer, deposition of a nitride layer, and formation of a second oxide layer.

11. The method of claim 10, wherein said step of forming a first oxide layer comprises thermal oxidation.

12. The method of claim 10, wherein said step of forming a first oxide layer comprises chemical vapor deposition.

13. The method of claim 10, wherein said step of forming a second oxide layer comprises thermal oxidation.

14. The method of claim 10, wherein said step of forming a second oxide layer comprises chemical vapor deposition.

15. The method of claim 1, wherein the dielectric layer is a layer of ON.

16. The method of claim 1, wherein the dielectric layer is a layer of oxide.

17. The method of claim 1, wherein the dielectric layer has a thickness within the range of approximately 70 to 180 Angstroms.

18. The method of claim 1, wherein the dielectric layer has a thickness within the range of approximately 120 to 140 Angstroms.

19. The method of claim 1, wherein the dielectric layer has a thickness of approximately 130 Angstroms.

20. The method of claim 1, wherein said step of forming a second polysilicon layer comprises chemical vapor deposition.

21. The method of claim 1, wherein said step of forming a second polysilicon layer comprises plasma deposition.

22. The method of claim 1, further comprising plasma etching of the second polysilicon layer to form the at least one control gate after said step of forming a second polysilicon layer.

23. The method of claim 1, wherein the at least one control gate has a thickness of approximately 300 to 1000 Angstroms.

24. The method of claim 1, wherein the at least one control gate has a thickness of approximately 500 Angstroms.

25. The method of claim 1, wherein said step of removing the plurality of nitride spacers comprises wet etching.

26. The method of claim 1, wherein said step of removing the plurality of nitride spacers comprises dry etching.

27. A method of forming split-gate transistors, comprising the steps of:

providing a substrate which has a plurality of isolation bars formed therein;

forming a tunneling oxide layer on the substrate between the isolation bars;

forming a first polysilicon layer on the tunneling oxide layer;

forming a plurality of nitride spacers, wherein each spacer is formed over one of the isolation bars, and wherein the plurality of spacers divides the first polysilicon layer into a plurality of U-shaped floating gates;

forming a plurality of polysilicon spacers on the nitride spacers;

removing the plurality of nitride spacers;

forming a dielectric layer on the floating gates; and

forming a second polysilicon layer on the dielectric layer, wherein the plurality of spacers divides the second polysilicon layer into a plurality of U-shaped control gates.

28. The method of claim 27, wherein said step of forming a tunneling oxide layer comprises thermal oxidation.

29. The method of claim 27, wherein said step of forming a tunneling oxide layer comprises chemical vapor deposition.

30. The method of claim 27, wherein the tunneling oxide layer has a thickness within the range of approximately 50 to 110 Angstroms.

31. The method of claim 27, wherein the tunneling oxide layer has a thickness within the range of approximately 70 to 100 Angstroms.

32. The method of claim 27, wherein the tunneling oxide layer has a thickness of approximately 80 Angstroms.

33. The method of claim 27, further comprising forming source and drain regions in the substrate in a direction orthogonal to said plurality of nitride spacers.

34. The method of claim 27, wherein said step of forming a first polysilicon layer comprises chemical vapor deposition.

35. The method of claim 27, wherein said step of forming a first polysilicon layer comprises plasma deposition.

36. The method of claim 27, wherein said step of forming a plurality of nitride spacers comprises defining trenches in the first polysilicon layer and filling the trenches with nitride.

37. The method of claim 27, wherein the floating gates have a thickness of approximately 200 to 1000 Angstroms.

38. The method of claim 27, wherein the floating gates have a thickness of approximately 500 Angstroms.

39. The method of claim 27, wherein the dielectric layer is a layer of ONO.

40. The method of claim 39, wherein said step of forming a dielectric layer comprises formation of a first oxide layer, deposition of a nitride layer, and formation of a second oxide layer.

41. The method of claim 27, wherein the dielectric layer is a layer of ON.

42. The method of claim 27, wherein the dielectric layer is a layer of oxide.

43. The method of claim 27, wherein the dielectric layer has a thickness within the range of approximately 120 to 140 Angstroms.

44. The method of claim 27, wherein the dielectric layer has a thickness of approximately 130 Angstroms.

45. The method of claim 27, wherein said step of forming a second polysilicon layer comprises chemical vapor deposition.

46. The method of claim 27, further comprising plasma etching of the second polysilicon layer to form the plurality of U-shaped control gates after said step of forming a second polysilicon layer.

47. The method of claim 27, wherein the control gates have a thickness of approximately 300 to 1000 Angstroms.

48. The method of claim 27, wherein the control gates have a thickness of approximately 500 Angstroms.

49. A method of forming split-gate transistors, comprising the steps of:

forming a first polysilicon layer on a substrate which has a plurality of isolation bars formed therein;

forming a plurality of trenches in the first polysilicon layer, wherein each trench is formed over one of the isolation bars in a direction parallel to the bars;

forming a plurality of nitride spacers by filling the plurality of trenches with nitride, wherein the plurality of spacers divides the first polysilicon layer into a plurality of U-shaped floating gates;

forming a plurality of polysilicon spacers on the nitride spacers;

removing the plurality of nitride spacers;

forming a dielectric layer on the floating gates; and

forming a second polysilicon layer on the dielectric layer, wherein the plurality of spacers divides the second polysilicon layer into a plurality of U-shaped control gates.

50. The method of claim 49, further comprising forming source and drain regions in the substrate in a direction orthogonal to said plurality of nitride spacers.

51. The method of claim 49, further comprising forming a tunneling oxide layer on the substrate prior to said step of forming a first polysilicon layer.

52. The method of claim 49, wherein said step of forming a plurality of trenches comprises defining the plurality of trenches using photolithography, and subsequently removing portions of the first polysilicon layer to form the plurality of trenches.

53. The method of claim 52, wherein said removal step comprises wet etching.

54. The method of claim 52, wherein said removal step comprises plasma etching.

55. The method of claim 52, wherein said removal step comprises reactive ion etching.

56. The method of claim 49, wherein said step of forming a plurality of nitride spacers comprises chemical vapor deposition.

57. The method of claim 49, wherein said step of forming a plurality of nitride spacers comprises plasma deposition.

58. The method of claim 49, wherein said step of forming a plurality of polysilicon spacers further comprises etching of the first polysilicon layer to form the plurality of U-shaped floating gates.

59. The method of claim 58, wherein said etching step comprises wet etching.

60. The method of claim 58, wherein said etching step comprises plasma etching.

61. The method of claim 58, wherein said etching step comprises reactive ion etching.

62. The method of claim 58, wherein the first polysilicon layer has a thickness within the range of 2000 to 3000 Angstroms.

63. The method of claim 58, wherein the first polysilicon layer has a thickness within the range of 2250 to 2750 Angstroms.

64. The method of claim 58, wherein the first polysilicon layer has a thickness of approximately 2500 Angstroms.

65. The method of claim 49, wherein the floating gates have a thickness of approximately 200 to 1000 Angstroms.

66. The method of claim 49, wherein the floating gates have a thickness of approximately 500 Angstroms.

67. The method of claim 49, wherein said step of forming a second polysilicon layer further comprises plasma etching of the second polysilicon layer to form the plurality of U-shaped control gates.

68. The method of claim 67, wherein the second polysilicon layer has a thickness within the range of 2000 to 3000 Angstroms.

69. The method of claim 67, wherein the second polysilicon layer has a thickness within the range of 2250 to 2750 Angstroms.

70. The method of claim 67, wherein the second polysilicon layer has a thickness of approximately 2500 Angstroms.

71. The method of claim 49, wherein the control gates have a thickness of approximately 300 to 1000 Angstroms.

72. The method of claim 49, wherein the control gates have a thickness of approximately 500 Angstroms.

73. The method of claim 49, further comprising formation of a passivation layer over the second polysilicon layer after the control gates have been formed.

74. The method of claim 73, wherein the passivation layer is a layer of silicon dioxide.

75. The method of claim 73, wherein the passivation layer is a layer of glass selected from the group consisting of BSG, PSG, and BPSG.